

IN THE CLAIMS

Please amend claims 31 and 34-36. All claims have been provided as a courtesy to the Examiner.

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31. (Amended) A memory device, comprising:
a memory array;
a register [configured] to store at least one bit indicating a suspend status of a
write operation; and
a control circuit coupled to said memory array and said register, said control
circuit [is configured] to update said register and to control the output of a status signal
representing said protection status of said data modification operation, and wherein said
control circuit includes:
a first state machine [configured] to update at least one of said bits
indicating said suspend status of said write operation in response to a suspend
signal, and
a second state machine coupled to said first state machine and
[configured] to control the output of said status signal in response to a status
request signal.

32. (Unchanged) The memory device of claim 31, wherein said write operation
represents a byte write operation.

33. (Unchanged) The memory device of claim 31, wherein said suspend signal
represents a byte write suspend command.

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1 34. (Amended) The memory device of claim 31, wherein said control circuit is
2 [configured] to receive a status request signal and said register is [configured] to output
3 said status signal in response to said status request signal, said status signal having a first
4 state to indicate said write operation is suspended and a second state to indicate said write
5 operation is not suspended.

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1 35. (Amended) The memory device of claim 35, further comprising:
2 at least one data input/output coupled to said control circuit, wherein the at least
3 one data input/output is [configured] to receive said status request signal from a processor
4 and to provide said status signal to said processor.

1 36. (Amended) The memory device of claim 31, further comprising:
2 a status output coupled to said register, wherein said status output is [configured]
3 to provide a second status signal if [when] said status output is polled, and wherein said
4 second status signal having a first state to indicate said write operation is suspended and a
5 second state to indicate said write operation is not suspended.

1 37. (Unchanged) The memory device of claim 31, wherein said status request signal
2 is a read status register command.